## CLAIMS

What is claimed is:

1. A method for testing a semiconductor device having at least one first sector of a first sector type and at least one second sector of a second sector type, comprising:

measuring at least one first time period related to erasing the first sector;

establishing at least a first test limit based at least in part on the first time period;

measuring at least one second time period related to erasing the second sector;

establishing at least a second test limit based at least in part on the second time period; and

using the first and second test limits, determining whether the device passes or fails an erase test.

2. The method of Claim 1, wherein the device comprises plural first sectors and plural second sectors, and the first test limit is based at least in part on an average of first time periods associated with respective first sectors and the second test limit is based at least in part on an average of second time periods associated with respective second sectors.

3. The method of Claim 1, further comprising measuring at least one third time period related to erasing the first sector and measuring at least one fourth time period related to erasing the second sector, the first and second time periods being erase time periods and the third and fourth time periods being APDE time periods, the first test limit being based at least partially on at least one of: the first and third time periods, the second test limit being based at least partially on at least one of: the second and fourth time periods.

4. The method of Claim 3, wherein the first test limit is based at least partially on both of the first and third time periods, and the second test limit is based at least partially on both of the second and fourth time periods.

5. The method of Claim 2, further comprising measuring at least third time periods related to erasing respective first sectors and measuring at least fourth time periods related to

erasing respective second sectors, the first and second time periods being erase time periods and the third and fourth time periods being APDE time periods, the first test limit being based at least partially on at least one of: the first and third time periods, the second test limit being based at least partially on at least one of: the second and fourth time periods.

6. The method of Claim 5, wherein the first test limit is based at least partially on both of the first and third time periods, and the second test limit is based at least partially on both of the second and fourth time periods.

7. The method of Claim 1, wherein the act of using includes determining, for each sector, whether the time period associated with the sector exceeds the test limit associated with the time period of the sector.

8. The method of Claim 1, further comprising executing at least one parameter test on the device.

9. The method of Claim 1, wherein the second sector is a boot sector.

10. A device for testing a semiconductor device having at least one first sector of a first sector type and at least one second sector of a second sector type, comprising:

means for measuring at least one first time period related to erasing the first sector;

means for establishing at least a first test limit based at least in part on the first time period;

means for measuring at least one second time period related to erasing the second sector;

means for establishing at least a second test limit based at least in part on the second time period; and

means for determining, using the first and second test limits, whether the device passes or fails an erase test.